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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,382	09/16/2003	Tomonori Kanai	4703-0101P	2172

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,382	KANAI ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on May 8, 2006 has been received and entered in the case.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 5 – 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Seshan (U. S. Pat. No. 6,686,659).

Regarding claim 5, Seshan discloses in e.g., Fig. 11 a semiconductor device (510; column 9, line 51) comprising:

- peripheral electrodes (502 at the edge) formed on a periphery of a semiconductor chip (500; column 8, line 64);
- internal electrodes (502 at the center) formed inside the peripheral electrodes on the semiconductor chip (see Fig. 11); and
- circuits (520; column 9, line 55) formed in the semiconductor chip,

- wherein the peripheral electrodes (502 at the edge) are connected to the circuits by an internal line (i.e., 515; column 9, line 65) covered by an insulating layer (320 and/or 322 or the uppermost insulating layer that contains the conductive layer 502; see Fig. 6, Fig. 11 and column 7, lines 28 – 34), the internal electrodes (502 at the center) are connected to the circuits and the peripheral electrodes by the internal line (see Fig. 11 and column 10, lines 31 – 37), and the internal electrodes (502 at the center) are also connected to rewired lines (e.g., 603; column 10, line 3), the rewired lines formed above the internal electrodes with an insulating layer (600; column 9, lines 3 – 4) therebetween, and at ends of the rewired lines formed area array electrodes (i.e., 604 in Fig. 11),
- said peripheral electrodes (502 at the edge) being formed within openings (the opening for the elements 502 in the insulating layer, i.e., 320 and/or 322 or the uppermost insulating layer that contains the conductive layer 502) provided in said insulating layer (see Fig. 6, Fig. 11 and column 7, lines 28 – 34).

Regarding claim 6, Seshan discloses in e.g., Fig. 11 a semiconductor device (510) comprising:

- peripheral electrodes (502 at the edge) formed on a periphery of a semiconductor chip (500);
- internal electrodes (502 at the center) formed inside the peripheral electrodes on the semiconductor chip (see Fig. 11);

- area array electrodes (604, 608 and 610) connected to selected one of the peripheral electrodes and the internal electrodes and formed on the semiconductor chip; and
- circuits (520; column 9, line 55) formed in semiconductor chip,
- wherein the peripheral electrodes (502 at the edge) are connected to the circuits by an internal line (i.e., 515; column 9, line 65) covered by an insulating layer (320 and/or 322 or the uppermost insulating layer that contains the conductive layer 502; see Fig. 6, Fig. 11 and column 7, lines 28 – 34), the internal electrodes (502 at the center) are connected to the circuits and the peripheral electrodes by the internal line (see Fig. 11 and column 10, lines 31 – 37), and the area array electrodes (604, 608 and 610) comprise first area array electrodes (604) connected to the internal electrodes (502 at the center) by rewired lines (603) and second area array electrodes (608 and 610) connected to the peripheral electrodes (502 at the edge) by rewired lines (607 and 609).
- said peripheral electrodes (502 at the edge) being formed within openings (the opening for the elements 502 in the insulating layer, i.e., 320 and/or 322 or the uppermost insulating layer that contains the conductive layer 502) provided in said insulating layer (see Fig. 6, Fig. 11 and column 7, lines 28 – 34).

Regarding claim 7, Seshan discloses in e.g., Fig. 11 the internal electrodes comprising a power supply terminal (column 9, lines 16 – 18).

Regarding claim 8, Seshan discloses in e.g., Fig. 11, column 1, lines 39 – 43 and column 9, lines 55 – 58 the peripheral electrodes not connected to the internal electrodes

being used as terminals for RF signals (since the circuit element 520 is radio frequency circuits, inherently, the input/output signals of the elements 502 at the edge are radio frequency signals).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seshan in view of Saito (U. S. Pat. No. 6,586,830).

Regarding claim 1, Seshan discloses in e.g., Fig. 6 and Fig. 11 a semiconductor device (500; column 8, line 64) comprising:

- peripheral electrodes (502 at the edge that are surrounded the other 502; column 9, line 18) formed on a periphery of a semiconductor chip (500; column 8, line 64);
- internal electrodes (502 at the center; column 9, line 18) formed inside the peripheral electrodes on the semiconductor chip (see e.g., Fig. 11); and
- circuits (520; column 9, lines 55 – 58) formed in the semiconductor chip,
- wherein the peripheral electrodes (502 at the edge) are
    - connected to the circuits by an internal line (i.e., 515; column 9, line 65), and

- the internal electrodes are connected to the circuits and the peripheral electrodes by the internal line (see e.g., Fig. 11 and column 10, lines 31 – 37),
- said internal line being covered by an insulating layer (320 and/or 322 or the uppermost insulating layer that contains the conductive layer 502; see Fig. 6, Fig. 11 and column 7, lines 28 – 34), and

- wherein the same signal (any input or output signal from or to the circuit element 520; column 9, lines 55 – 58) is either an input and/or output either to or from both the internal electrodes and the peripheral electrodes (since the elements 502 at the center and 502 at the edge are coupled together by an internal trace 515, the elements 502 at the center and 502 at the edge receive same signal from the circuit element 520. see Fig. 11 and column 10, lines 31 – 37), and
- wherein rewiring (514; column 9, line 64) is connected to either the peripheral electrodes, or to the internal electrodes (see e.g., Fig. 11),
- said peripheral electrodes (502 at the edge) being formed within an opening (the opening for the elements 502 in the insulating layer, i.e., 320 and/or 322 or the uppermost insulating layer that contains the conductive layer 502) provided in said insulating layer (see Fig. 6, Fig. 11 and column 7, lines 28 – 34).

Seshan does not disclose a wire bonding. Saito teaches in e.g., Fig. 12 a wire (29; column 9, line 20) being connected to peripheral electrodes (4; column 9, lines 22 and 23) connecting to external terminals (14; column 9, lines 22 and 23) using wire bonding

(see e.g., Fig. 12). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the wire bonding of Saito as the specific bonding connection to connect the peripheral electrodes to the external terminals of Seshan as taught by Saito to absorb a mechanical stress (column 2, lines 44 – 67).

Regarding claim 3, Seshan discloses in e.g., Fig. 11 the internal electrodes comprising a power supply terminal (column 9, lines 16 – 18).

Regarding claim 4, Seshan discloses in e.g., Fig. 11, column 1, lines 39 – 43 and column 9, lines 55 – 58 the peripheral electrodes not connected to the internal electrodes being used as terminals for RF signals (since the circuit element 520 is radio frequency circuits, inherently, the input/output signals of the elements 502 at the edge are radio frequency signals).

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seshan and Saito as applied to claim 1 above, and further in view of Arnold et al. (U. S. Pat. No. 4,521,449).

Seshan and Saito disclose the claimed invention except for the side of the internal electrodes being smaller than the peripheral electrodes. Arnold et al. teaches in Fig. 2 the side of internal electrodes (24; column 5, lines 14 and 15) being smaller than peripheral electrodes (42; column 3, line 50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Seshan by using the small size of the internal electrodes of Arnold et al. into the internal electrodes of Seshan and Saito as taught by Arnold et al. The ordinary artisan would have been motivated to further modify Seshan in the manner described above for at least the purpose of providing

the density of vias to be less dense than the pads of the I/O connections to the device (column 3, lines 40 – 43).

Response to Arguments

6. Applicant's arguments filed on May 8, 2006 have been fully considered but they are either moot in light of the new grounds of rejection or are not persuasive.

(A) Response to the Claim Rejections under 35 USC § 102(e)

On page 7, applicant argues that terminal 504 of Seshan is different from the peripheral electrodes in the present invention. As explained in the previous Office action, this argument is not persuasive because the "peripheral electrodes" in the rejected claim 1 are not specifically defined in the claim or in the specification of instant invention. Thus, a reasonable interpretation of the term "peripheral electrodes" includes the structure taught by Seshan. In other words, the terminals 502 at the edge of Seshan are located at the peripheral area in the chip 500 than the terminals 502 at the center and connected to the solder ball 506. Thus, the terminals 502 at the edge of Seshan anticipate the term "peripheral electrodes".

Furthermore, applicant argues that the newly amended claims 5 and 6 are not anticipated by Seshan. This argument is not persuasive because the newly amended claims 5 and 6 are clearly anticipated by Seshan (see paragraph two of this Office action for detail.)

For the above reasons, the rejection is maintained.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Monday, June 19, 2006

KENNETH PARKER
SUPERVISORY PATENT EXAMINER